

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-15. canceled

16. (currently amended): A semiconductor integrated circuit comprising:
a plurality of analog/digital converting circuits (11) operated in parallel for sequentially
converting an analog image signal to a digital image signal;
a multi-phase clock signal generating circuit (12) for generating multi-phase clock signals
to be used for periodically operating said plurality of analog/digital converting circuits (11) in a
certain order; and
a control circuit (20) for controlling said multi-phase clock signal generating circuit (12)
to change at least one of a period and an order of operating said plurality of analog/digital
converting circuits (11).

17. (currently amended): The semiconductor integrated circuit according to claim 16-1,
wherein said control circuit (20) controls said multi-phase clock signal generating circuit (12)
based on a number of pixels included in one frame of the digital image signal and a number of
said plurality of analog/digital converting circuits such that said plurality of analog/digital
converting circuits (11) never performs conversion in a same period and in a same order with
respect to pixels for at least successive two frames.

18. (currently amended): The semiconductor integrated circuit according to claim 17-2,
wherein said control circuit (20) controls said multi-phase clock signal generating circuit (12)
based on the number of pixels included in one frame of the digital image signal and the number
of said plurality of analog/digital converting circuits such that said plurality of analog/digital
converting circuits (11) never performs conversion in a same period and in a same order with
respect to pixels for successive N frames where the number of said plurality of analog/digital
converting circuits is N.

19. (currently amended): The semiconductor integrated circuit according to claim 161, wherein said control circuit (20) controls said multi-phase clock signal generating circuit (12) based on an output of a pseudorandom number generating circuit for generating at least N integers where the number of said plurality of analog/digital converting circuits is N so as to shift timing of sampling operation of said plurality of analog/digital converting circuits (11).

20. (currently amended): The semiconductor integrated circuit according to claim 161, wherein said multi-phase clock signal generating circuit (12) counts pulses of a master clock signal and stores counter values to be used for generating the multi-phase clock signals; and

 said control circuit (20) controls said multi-phase clock signal generating circuit (12) by changing the counter values stored in said multi-phase clock signal generating circuit (12) at predetermined timing.

21. (currently amended): The semiconductor integrated circuit according to claim 161, wherein said multi-phase clock signal generating circuit (12) counts pulses of a master clock signal and stores counter values to be used for generating the multi-phase clock signals; and

 said control circuit (20) controls said multi-phase clock signal generating circuit (12) by changing the counter values stored in said multi-phase clock signal generating circuit (12) at predetermined timing based on a counter value obtained by counting the pulses of the master clock signal.

22. (currently amended): The semiconductor integrated circuit according to claim 161, wherein said control circuit (20) outputs a clock signal obtained by suppressing a predetermined number of pulses included in a master clock signal; and

 said multi-phase clock signal generating circuit (12) generates said multi-phase clock signals based on counter values obtained by counting pulses of the clock signal outputted from said control circuit (20).

23. (currently amended): The semiconductor integrated circuit according to claim 227, wherein said control circuit (20) outputs the clock signal obtained by suppressing the predetermined number of pluses included in the master clock signal in a blanking period of the digital image signal.

24. (currently amended): A semiconductor integrated circuit comprising:

an analog/digital converting circuit (11) for converting an analog image signal to a digital image signal by sequentially switching between a plurality of circuit elements;

a first control circuit (31, 71) for controlling said analog/digital converting circuit (11) to periodically arrange said plurality of circuit elements in a certain order; and

a second control circuit (40, 80) for controlling said first control circuit (31, 71) to change at least one of a period and an order of arranging said plurality of circuit elements.

25. (currently amended): The semiconductor integrated circuit according to claim 249, wherein said second control circuit (40, 80) controls said first control circuit (31, 71) based on a number of pixels included in one frame of the digital image signal and a number of said plurality of circuit elements such that said analog/digital converting circuit (11) never arranges said plurality of circuit elements in a same period and in a same order with respect to pixels for at least successive two frames.

26. (currently amended): The semiconductor integrated circuit according to claim 2510, wherein said second control circuit (40, 80) controls said first control circuit (31, 71) based on the number of pixels included in one frame of the digital image signal and the number of said plurality of circuit elements such that said analog/digital converting circuit never arranges said plurality of circuit elements in the same period and in the same order with respect to pixels for successive N frames where a number of said circuit elements is N.

27. (currently amended): The semiconductor integrated circuit according to claim 249, wherein said first control circuit (31) counts a master clock signal and stores counter values to be used for generating multi-phase control signals for controlling said analog/digital converting circuit (11); and

said second control circuit (40) controls said first control circuit (31) by changing the counter values stored in said first control circuit at predetermined timing. ~~13. The semiconductor integrated circuit according to claim 9, wherein said first control circuit (31) counts a master clock signal and stores counter values to be used for generating multi-phase control signals for controlling said analog/digital converting circuit (11); and~~

~~said second control circuit (40) controls said first control circuit (31) by changing the counter values stored in said first control circuit at a predetermined interval based on a counter value obtained by counting a master clock signal.~~

28. (currently amended): The semiconductor integrated circuit according to claim 249, wherein said second control circuit (80) outputs a clock signal obtained by suppressing a predetermined number of pulses included in a master clock signal; and

~~said first control circuit (71) generates multi-phase control signals for controlling said analog/digital converting circuit (41) based on counter values obtained by counting the clock signal outputted from said second control circuit (80).~~

29. (currently amended): The semiconductor integrated circuit according to claim 2814, wherein said second control circuit (80) outputs the clock signal obtained by suppressing the predetermined number of pulses included in the master clock signal in a blanking period of the digital image signal.

30. (new): The semiconductor integrated circuit according to claim 24, wherein said first control circuit counts a master clock signal and stores counter values to be used for generating multi-phase control signals for controlling said analog/digital converting circuit; and

said second control circuit controls said first control circuit by changing the counter values stored in said first control circuit at a predetermined interval based on a counter value obtained by counting a master clock signal.